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EXAMINER	
JEFFERSON, QUOVAUNDA	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,578	BOWER, ROBERT W.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *various*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

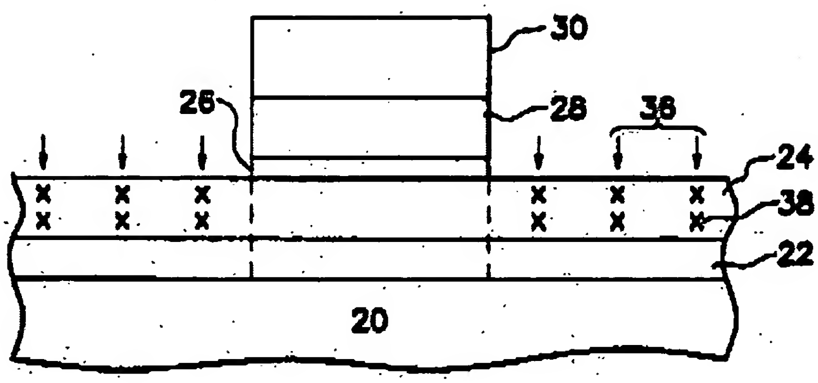
DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Yue, US Patent 5,244,819. See Yue Figure.



YUE FIGURE

Regarding claim 1, Yue teaches a multilayered material for fabrication of a nanodevice, comprising of a device layer **28** and a substrate layer **20, 22, 24** adjacent said device layer, wherein said substrate layer comprises a diffusion layer **24** having a collection region **28** adapted for capture of hydrogen (column 1, line 30 and column 3, lines 4-6).

Regarding claim 2, Yue teaches a material as recited in claim 1, wherein said substrate layer further comprises an insulator layer **26** between said device layer and said diffusion layer.

Regarding claim 3, Yue teaches a material as recited in claim 1, wherein said collection region is a heavily doped region for capture of hydrogen (column 1, line 30 and column 3, lines 4-6).

Regarding claim 4, Yue teaches a material as recited in claim 1, wherein said collection region is a getter/acceptor region for capture of hydrogen (column 1, line 52-53).

Regarding claim 5, Yue teaches a material as recited in claim 1, wherein said device layer comprises a material having at least a portion that has been optimized for fabricating said nanodevice.

Regarding claim 6, Yue teaches a material as recited in claim 2, wherein said insulator layer comprises a material that provides a high degree of electrical and thermal insulation between the diffusion layer and the device layer (column 2, line 46).

Regarding claim 7, Yue teaches a material as recited in claim 1, wherein said diffusion layer comprises a material optimized for a high rate of diffusion of hydrogen there through (column 3).

Claims 8-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Okonogi, US Patent 6,323,109. See Okonogi Figures 1A-1E.

FIG. 1A
(PRIOR ART)

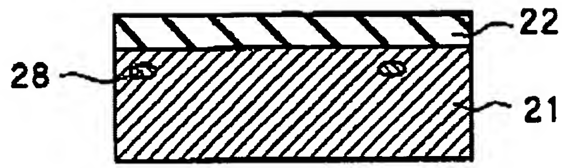


FIG. 1B
(PRIOR ART)

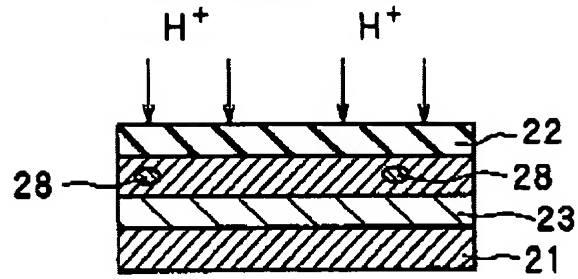


FIG. 1C
(PRIOR ART)

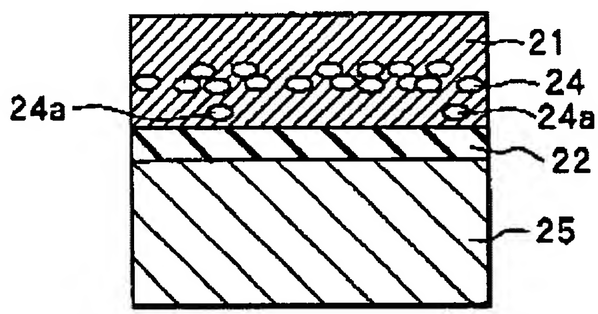


FIG. 1D
(PRIOR ART)

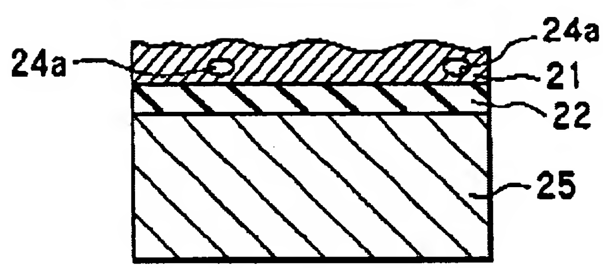
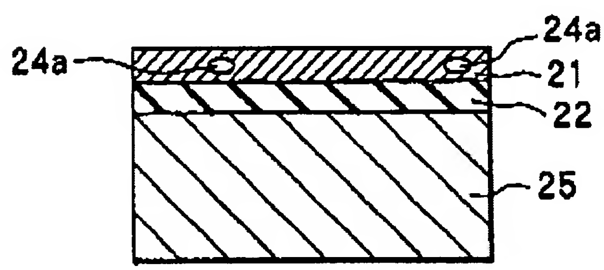


FIG. 1E
(PRIOR ART)



<u>OKONOGI</u> FIGURES

Regarding claim 8, Okonogi teaches a multilayered material for fabrication of a nanodevice, comprising of a device layer **25** and a substrate layer **21** adjacent said device layer, wherein said substrate layer comprises a diffusion layer **23** having a collection region adapted for capture of hydrogen, wherein said substrate layer further comprises an insulator layer **22** between said device layer and said diffusion layer.

Regarding claim 9, Okonogi teaches a material as recited in claim 8, wherein said collection region is a heavily doped region for capture of hydrogen (column 1, lines 27-30).

Regarding claim 10, Okonogi teaches a material as recited in claim 8, wherein said collection region is a getter/acceptor region for capture of hydrogen.

Regarding claim 11, Okonogi teaches a material as recited in claim 8, wherein said device layer comprises a material having at least a portion that has been optimized for fabricating said nanodevice.

Regarding claim 12, Okonogi teaches a material as recited in claim 8, wherein said insulator layer comprises a material that provides a high degree of electrical and thermal insulation between the diffusion layer and the device layer.

Regarding claim 13, Okonogi teaches a material as recited in claim 8, wherein said diffusion layer comprises a material optimized for a high rate of diffusion of hydrogen there through.

Claims 14-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Henley et al, US Patent 6,083,324. See Henley Figure 9A.

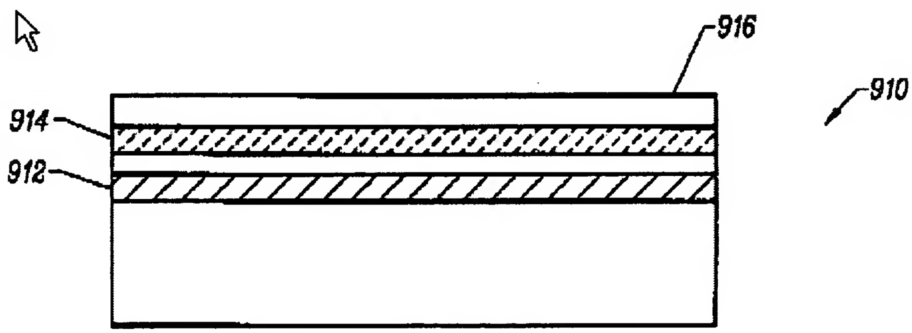


FIG. 9A

HENLEY FIGURE

Regarding claim 14, Henley teaches a multilayered material for use in fabrication of a nanodevice, comprising of a device layer **916**, an insulator layer **914** adjacent said device layer, and a diffusion layer having a collection region **912** adapted for capture of hydrogen adjacent said insulator layer.

Regarding claim 15, Henley teaches a material as recited in claim 14, wherein said collection region is a heavily doped region for capture of hydrogen (column 4, lines 12-21).

Regarding claim 16, Henley teaches a material as recited in claim 14, wherein said collection region is a getter/acceptor region for capture of hydrogen.

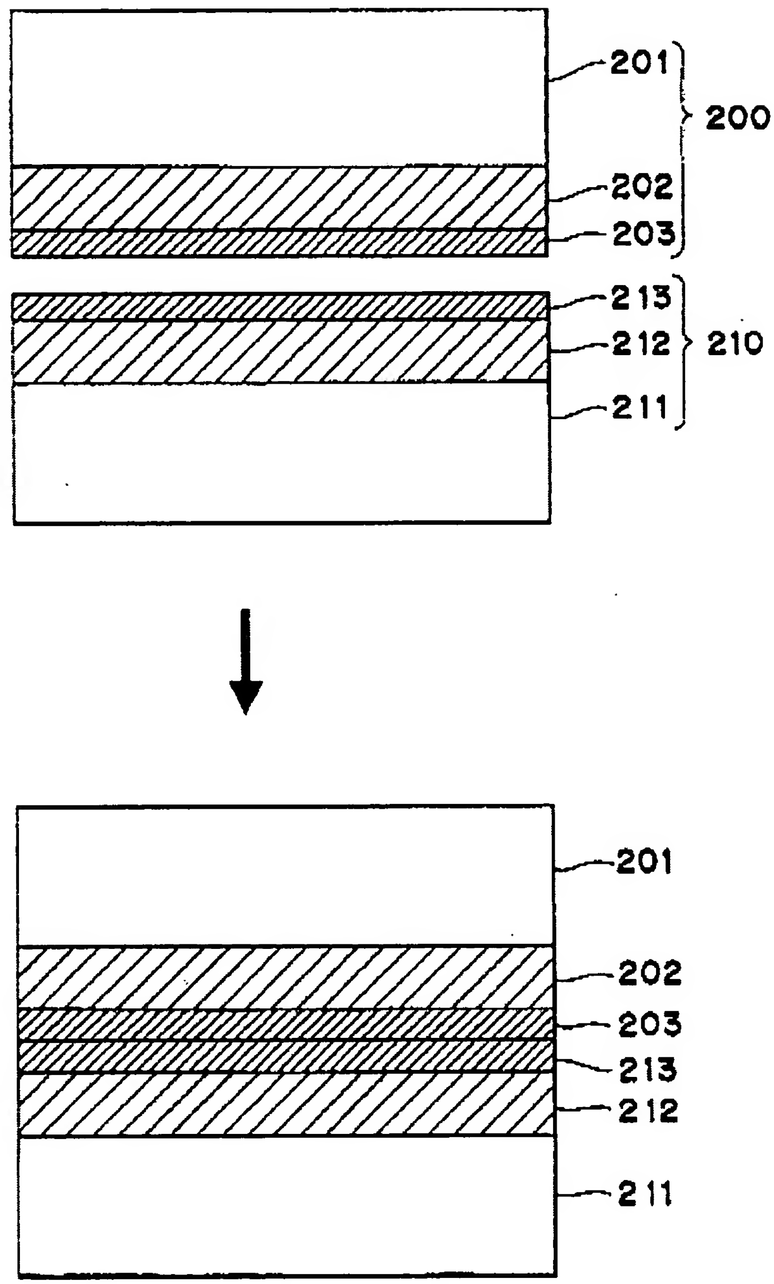
Regarding claim 17, Henley teaches a material as recited in claim 14, wherein said device layer comprises a material having at least a portion that has been optimized for fabricating said nanodevice (column 5, lines 60-67).

Regarding claim 18, Henley teaches a material as recited in claim 14, wherein said insulator layer comprises a material that provides a high degree of electrical and thermal insulation between the diffusion layer and the device layer.

Regarding claim 19, Henley teaches a material as recited in claim 14, wherein said diffusion layer comprises a material optimized for a high rate of diffusion of hydrogen there through.

Claims 20-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Yonehara et al, US Patent 5,453,394. See Yonehara Figures 2.

FIG. 2



<u>YONEHARA</u> FIGURE

Regarding claim 20, Yonehara teaches a multilayered material for use in fabrication of a nanodevice, comprising of a layer of material **210** for device fabrication, a layer of insulator material **213**, and a layer of material **203, 213** though which hydrogen can diffuse at a high rate and having a collection region adapted for capture of hydrogen, wherein said layer of insulator material is disposed between said layer of material for device fabrication and said collection region.

Regarding claim 21, Yonehara teaches a material as recited in claim 20, wherein said collection region is a heavily doped region for capture of hydrogen (column 7, lines 29-34).

Regarding claim 22, Yonehara teaches a material as recited in claim 20, wherein said diffusion layer has a getter/acceptor region for capture of hydrogen.

Regarding claim 23, Yonehara teaches a material as recited in claim 20, wherein said device layer comprises a material having at least a portion that has been optimized for fabricating said nanodevice.

Regarding claim 24, Yonehara teaches a material as recited in claim 20, wherein said insulator layer provides a high degree of electrical and thermal insulation between the diffusion layer and the device layer.

Regarding claim 25, Yonehara teaches a material as recited in claim 20, wherein said diffusion layer comprises a material optimized for a high rate of diffusion of hydrogen there through.

Regarding claim 26, Yonehara teaches a multilayered material for use in fabrication of a nanodevice, comprising of a layer of material **210** for device fabrication, said material having at least a portion that has been optimized for fabricating said nanodevice, a layer of material **203, 213** though which hydrogen can diffuse at a high rate and having a collection region adapted for capture of hydrogen, said collection region comprising a heavily doped region or a getter/acceptor region (column 7, lines 27-34), wherein said diffusion layer comprises a material optimized for a high rate of diffusion of hydrogen there through; and a layer of insulator material, wherein said insulator layer provides a high degree of electrical and thermal insulation between the diffusion layer and the device layer (columns 8 and 9), wherein the insulator layer is disposed between the device layer and the diffusion layer .

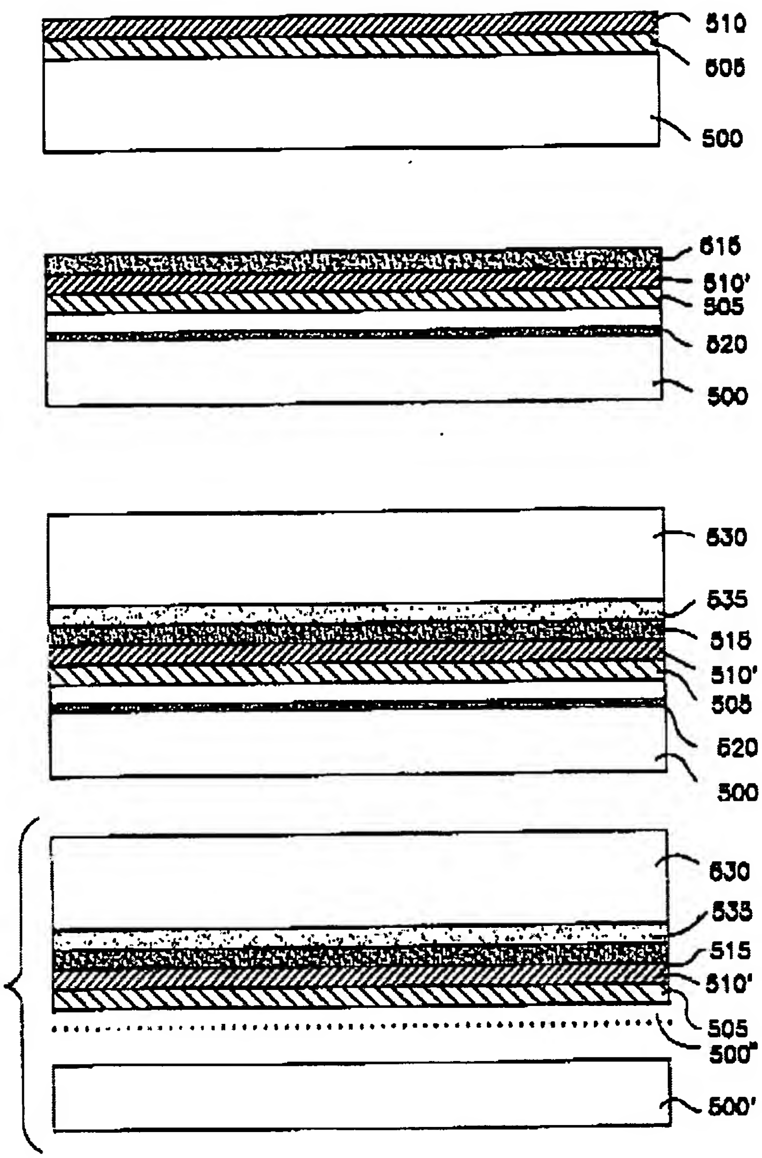
Claims 29-36 and 38-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Srikrishnan, US Patent 5,882,987. See Srikrishnan Figures.

FIG. 5A

FIG. 5B

FIG. 5C

FIG. 5D



SRIKRISHNAN FIGURE

Regarding claim 29, Srikrishnan teaches a method of fabricating a multilayered material for use in making a nanodevice, comprising of providing a wafer **500** having at least a portion **510** that has been optimized for making said nanodevice, implanting said

wafer with hydrogen to a depth **520** associated with a thickness to remain after an ion cut, and bonding said wafer to a substrate layer **530**, said substrate layer comprising a diffusion layer having a collection region adapted for capture of hydrogen (column 1, lines 30-33).

Regarding claim 30, Srikrishnan teaches a method as recited in claim 29, wherein said substrate layer further comprises an insulator layer **535** bonded to said diffusion layer.

Regarding claim 31, Srikrishnan teaches a method as recited in claim 29, wherein said collection region is a heavily doped region for capture of hydrogen (column 1, lines 30-33).

Regarding claim 32, Srikrishnan teaches a method as recited in claim 29, wherein said collection region is a getter/acceptor region for capture of hydrogen.

Regarding claim 33, Srikrishnan teaches a method as recited in claim 29, further comprising ion cutting said wafer so as to leave a device layer bonded to the substrate layer.

Regarding claim 34, Srikrishnan teaches a method as recited in claim 30, wherein said substrate layer is formed according to the steps comprising:

creating hydrogen getters in said collection region; and bonding the insulator layer to a surface of the diffusion layer adjacent the collection region.

Regarding claim 35, Srikrishnan teaches a method as recited in claim 30, wherein said substrate layer is formed according to the steps comprising of bonding the insulator layer to a surface of the diffusion layer adjacent the collection region; and creating hydrogen getters in said collection region beneath said insulator layer.

Regarding claim 36, Srikrishnan teaches a method as recited in claim 29, further comprising ion cutting said wafer so as to leave a device layer bonded to the substrate layer (Figure 5D).

Regarding claim 38, Srikrishnan teaches a method of fabricating a multilayered material for use in making a nanodevice, comprising of providing a wafer **500** having at least a portion **510** that has been optimized for making said nanodevice, implanting said wafer with hydrogen to a depth **520** associated with a thickness to remain after an ion cut, and bonding said wafer to a substrate layer **530**, said substrate layer comprising a diffusion layer having a collection region adapted for capture of hydrogen (column 1, lines 30-33), said substrate comprising an insulator layer **515** bonded to said diffusion layer.

Regarding claim 39, Srikrishnan teaches a method as recited in claim 38, wherein said collection region is a heavily doped region for capture of hydrogen (column 1, lines 30-33).

Regarding claim 40, Srikrishnan teaches a method as recited in claim 38, wherein said collection region is a getter/acceptor region for capture of hydrogen.

Regarding claim 41, Srikrishnan teaches a method as recited in claim 38, further comprising ion cutting said wafer so as to leave a device layer bonded to the substrate layer.

Regarding claim 42, Srikrishnan teaches a method as recited in claim 38, wherein said substrate layer is formed according to the steps comprising of creating hydrogen getters in said collection region, and bonding the insulator layer to a surface of the diffusion layer adjacent the collection region.

Regarding claim 43, Srikrishnan teaches a method as recited in claim 38, wherein said substrate layer is formed according to the steps comprising of bonding the insulator layer to a surface of the diffusion layer adjacent the collection region, and creating hydrogen getters in said collection region beneath said insulator layer.

Claims 45-50, 51-56, and 58-62 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato, US Patent 5,854,123. See Sato Figures.

FIG. 2B

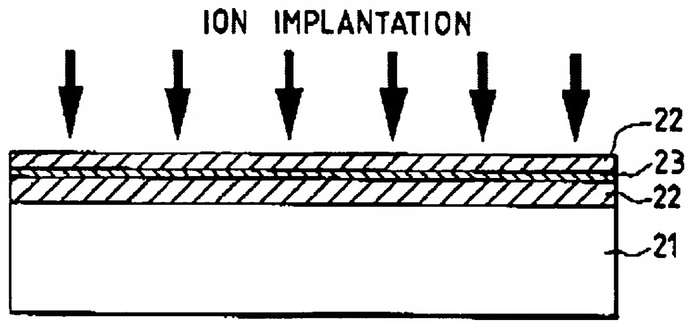


FIG. 8C

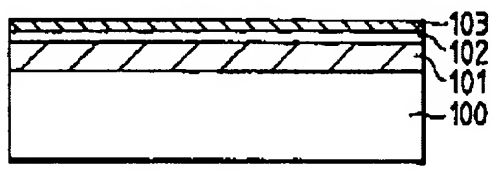


FIG. 8D

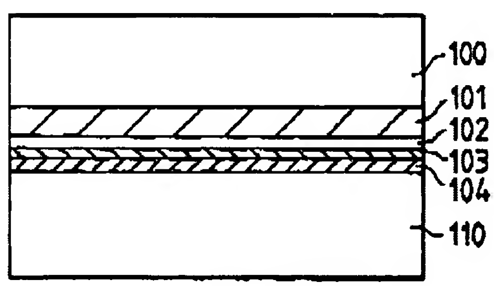
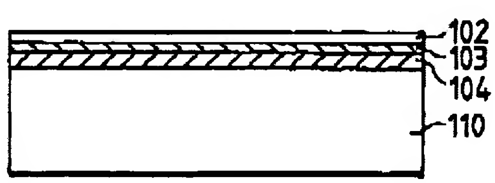


FIG. 8E



SATO FIGURES

Regarding claim 45, Sato teaches a method of fabricating a multilayered material for use in making a nanodevice, comprising of providing a wafer **21** having at least a portion **22** that has been optimized for making said nanodevice, implanting said wafer with hydrogen to a depth **23** associated with a thickness to remain after an ion cut (Figure 2B and column 17, lines 10-14), bonding said wafer to a substrate layer **110**, said substrate layer comprising a diffusion layer having a collection region adapted for capture of hydrogen, said substrate layer comprising an insulator layer **104** bonded to said diffusion layer, and ion cutting said wafer so as to leave a device layer **102** bonded to the substrate layer (Figures 8D, 8E, and column 2, lines 27-49).

Regarding claim 46, Sato teaches a method as recited in claim 45, wherein said collection region is a heavily doped region for capture of hydrogen (column 2, lines 27-49).

Regarding claim 47, Sato teaches a method as recited in claim 45, wherein said collection region is a getter/acceptor region for capture of hydrogen.

Regarding claim 48, Sato teaches a method as recited in claim 45, further comprising ion cutting said wafer so as to leave a device layer bonded to the substrate layer.

Regarding claim 49, Sato teaches a method as recited in claim 45, wherein said substrate layer is formed according to the steps comprising of creating hydrogen getters in said collection region, and bonding the insulator layer to a surface of the diffusion layer adjacent the collection region.

Regarding claim 50, Sato teaches a method as recited in claim 45, wherein said substrate layer is formed according to the steps comprising of bonding the insulator layer to a surface of the diffusion layer adjacent the collection region, and creating hydrogen getters in said collection region beneath said insulator layer.

Regarding claim 52, Sato teaches a method of fabricating a multilayered material for use in making a nanodevice, comprising of providing a wafer **21** having at least a portion **22** that has been optimized for making said nanodevice (Figure 2B), implanting said wafer with hydrogen to a depth **23** associated with a thickness to remain after an ion cut, forming a diffusion layer **110** having a region for collecting hydrogen, bonding said diffusion layer to an insulator layer **104**, bonding said insulator layer to said wafer **100** and ion cutting said wafer so as to leave a device layer bonded to the substrate layer (Figure 8D, 8E, and column 2, lines 27-49, and column 17, lines 10-14).

Regarding claim 53, Sato teaches a method as recited in claim 52, wherein said collection region is a heavily doped region for capture of hydrogen (column 2, lines 27-49).

Regarding claim 54, Sato teaches a method as recited in claim 52, wherein said collection region is a getter/acceptor region for capture of hydrogen.

Regarding claim 55, Sato teaches a method as recited in claim 52, wherein said substrate layer is formed according to the steps comprising of creating hydrogen getters in said collection region, and bonding the insulator layer to a surface of the diffusion layer adjacent the collection region.

Regarding claim 56, Sato teaches a method as recited in claim 52, wherein said substrate layer is formed according to the steps comprising of bonding the insulator layer to a surface of the diffusion layer adjacent the collection region and creating hydrogen getters in said collection region beneath said insulator layer.

Regarding claim 58, Sato further teaches a method of fabricating a multilayered material for use in making a nanodevice, comprising of providing a wafer **21** having at least a portion **22** that has been optimized for making said nanodevice, implanting said wafer with hydrogen to a depth **23** associated with a thickness to remain after an ion cut (column 17, lines 10-14), forming a diffusion layer **110** having a region for collecting hydrogen (column 2, lines 27-49) bonding said diffusion layer to an insulator layer **104**, bonding said insulator layer to said wafer **101**, ion cutting said wafer so as to leave a

device layer bonded to the substrate layer (Figure 8D) and planarizing said device layer (Figure 8E).

Regarding claim 59, Sato teaches a method as recited in claim 58, wherein said collection region is a heavily doped region for capture of hydrogen.

Regarding claim 60, Sato teaches a method as recited in claim 58, wherein said collection region is a getter/acceptor region for capture of hydrogen.

Regarding claim 61, Sato teaches a method as recited in claim 58, wherein said substrate layer is formed according to the steps comprising of creating hydrogen getters in said collection region, and bonding the insulator layer to a surface of the diffusion layer adjacent the collection region.

Regarding claim 62, Sato teaches a method as recited in claim 58, wherein said substrate layer is formed according to the steps comprising of bonding the insulator layer to a surface of the diffusion layer adjacent the collection region, and creating hydrogen getters in said collection region beneath said insulator layer.

Claims 64-77 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsui et al, US Patent 6,191,007. See Matsui Figures.

FIG.1A

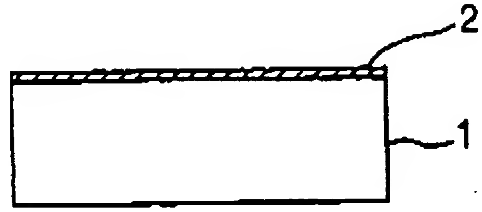


FIG.1B

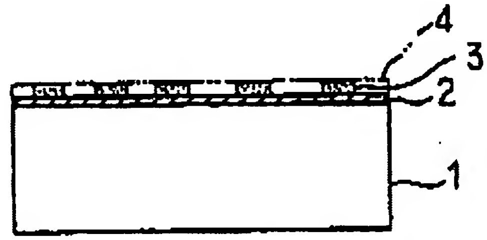


FIG.1C

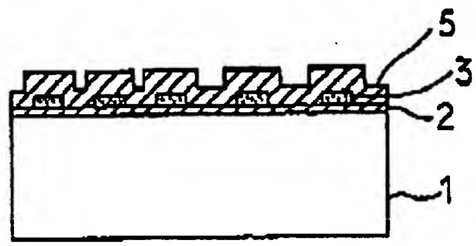


FIG.1D

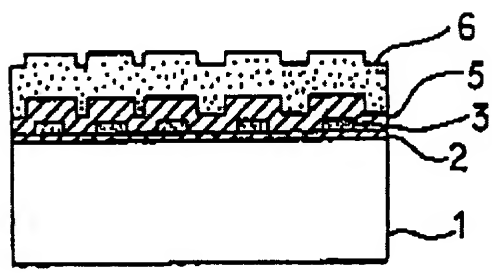
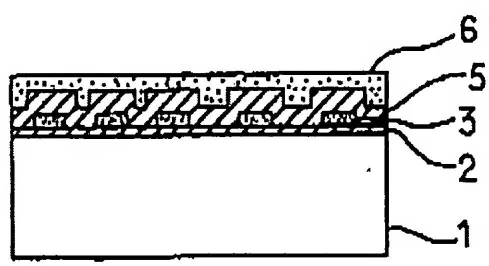


FIG.1E



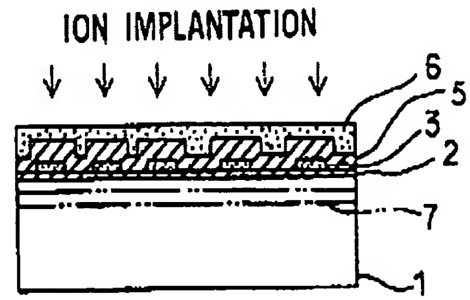


FIG. 2A

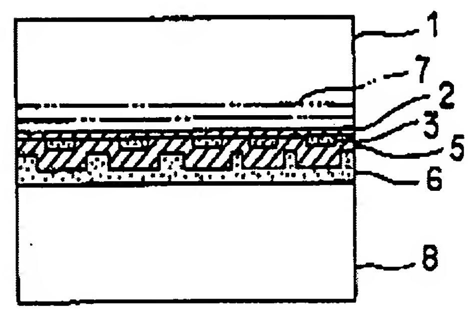


FIG. 2B

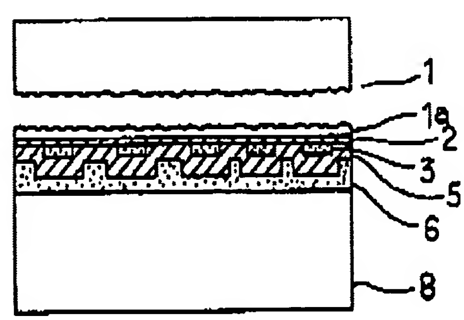


FIG. 2C

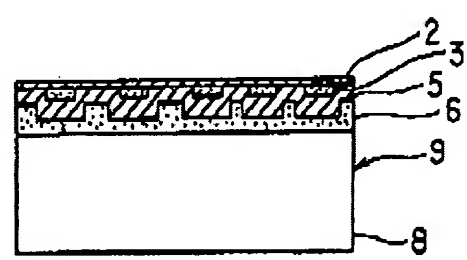


FIG. 2D

FIG. 3A

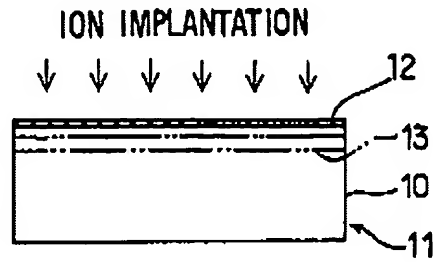


FIG. 3B

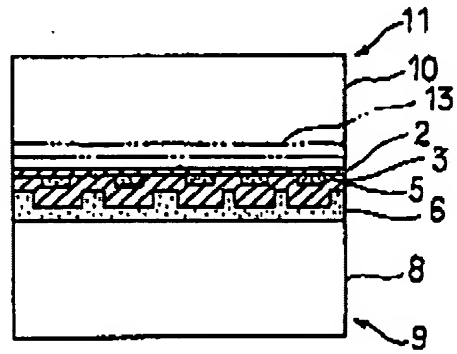


FIG. 3C

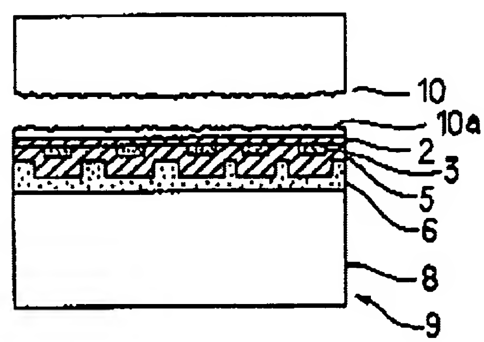


FIG. 3D

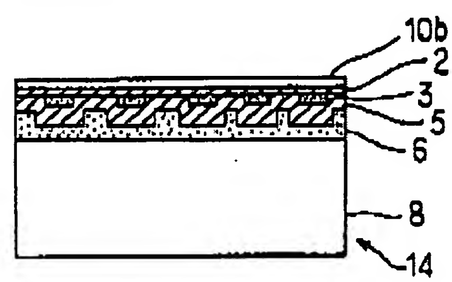


FIG. 56A

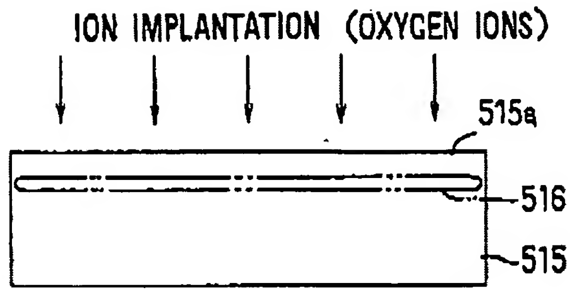


FIG. 56B

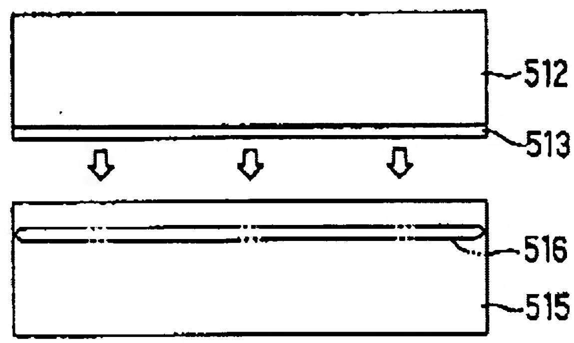


FIG. 56C

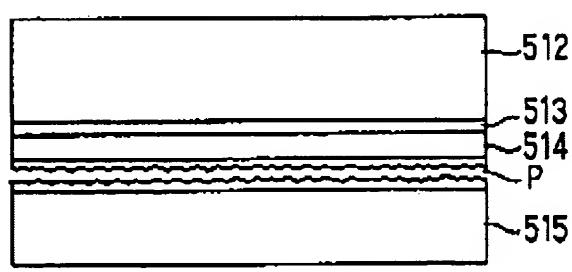


FIG. 56D

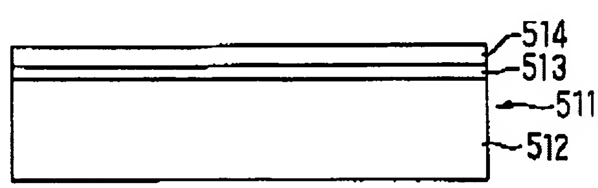
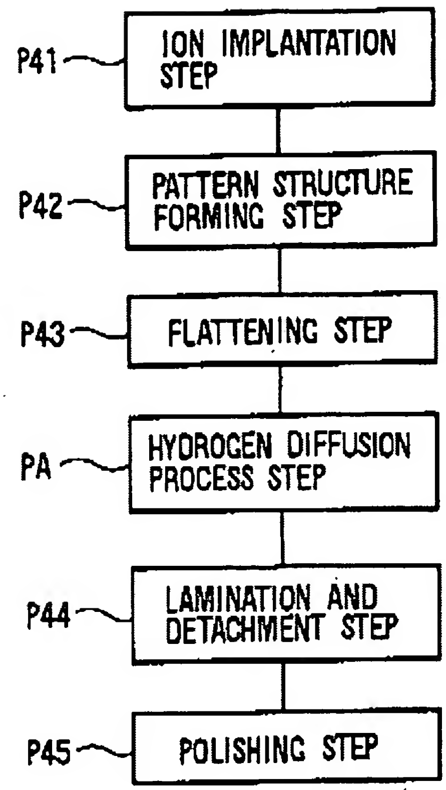


FIG. 55



<u>MATSUI</u> FIGURES

Regarding claim 64, Matsui teaches a method of fabricating. a nanodevice, comprising providing a wafer **1** having at least a portion **3** that has been optimized for making said nanodevice, implanting said wafer with hydrogen to a depth associated with a thickness to remain after an ion cut (Figure 2A), forming a diffusion layer having a region for collecting hydrogen (Figure 56A), bonding said diffusion layer to an insulator layer (Figure 56B), bonding said insulator layer to said wafer **512** (Figure 56B), ion

cutting said wafer so as to leave a device layer bonded to the substrate layer (Figure 2C), planarizing said device layer (Figure 2D), bonding said device layer to a 3-d stack or handle, injecting and diffusing hydrogen into said collection region (Figure 55), and ion cutting said diffusion layer at said collection region (Figure 55).

Regarding claim 65, Matsui teaches a method as recited in claim 64, wherein said collection region is a heavily doped region for capture of hydrogen.

Regarding claim 66, Matsui teaches a method as recited in claim 64, wherein said collection region is a getter/acceptor region for capture of hydrogen.

Regarding claim 67, Matsui teaches a method as recited in claim 64, wherein said substrate layer is formed according to the steps comprising of creating hydrogen getters in said collection region, and bonding the insulator layer to a surface of the diffusion layer adjacent the collection region.

Regarding claim 68, Matsui teaches a method as recited in claim 64, wherein said substrate layer is formed according to the steps comprising of bonding the insulator layer to a surface of the diffusion layer adjacent the collection region, and creating hydrogen getters in said collection region beneath said insulator layer.

Regarding claim 69, Matsui teaches a method as recited in claim 64, further comprising of removing said remaining diffusion layer and insulator layer.

Regarding claim 70, Matsui teaches a method of fabricating a nanodevice, comprising of providing a wafer **1** having at least a portion **3** that has been optimized for making said nanodevice, implanting said wafer with hydrogen to a depth associated with a thickness to remain after an ion cut (Figure 2A), bonding a diffusion layer to an insulator layer (Figure 56B), said diffusion layer having a region for collecting hydrogen; bonding said insulator layer **513** to said wafer **512**, ion cutting said wafer so as to leave a device layer bonded to the substrate layer (Figure 2C), planarizing said device layer (Figure 2D), bonding said device layer to a 3-d stack or handle (Figure 3B), injecting and diffusing hydrogen into said heavily doped region, ion cutting said diffusion layer at said heavily doped region, and removing said remaining diffusion layer and insulator layer (Figure 55 and Figure 56D).

Regarding claim 71, Matsui teaches a method as recited in claim 70, wherein said collection region is a heavily doped region for capture of hydrogen.

Regarding claim 72, Matsui teaches a method as recited in claim 70, wherein said collection region is a getter/acceptor region for capture of hydrogen.

Regarding claim 73, Matsui teaches a method as recited in claim 70, further comprising ion cutting said wafer so as to leave a device layer bonded to the substrate layer.

Regarding claim 74, Matsui teaches a method as recited in claim 70, wherein said substrate layer is formed according to the steps comprising of creating hydrogen getters in said collection region, and bonding the insulator layer to a surface of the diffusion layer adjacent the collection region.

Regarding claim 75, Matsui teaches a method as recited in claim 70, wherein said substrate layer is formed according to the steps comprising of bonding the insulator layer to a surface of the diffusion layer adjacent the collection region, and creating hydrogen getters in said collection region beneath said insulator layer.

Regarding claim 76, Matsui teaches a method as recited in claim 34, 35, 42, 43, 49, 50, 55, 56, 61, 62, 67, 68, 74 or 75, wherein said hydrogen getters are created by atomic injection (column 56, lines 29-30).

Regarding claim 77, Matsui teaches a method as recited in claim 34, 35, 42, 43, 49, 50, 55, 56, 61, 62, 67, 68, 74 or 75, wherein said hydrogen getters are created by plasma injection (column 87, lines 26-28).

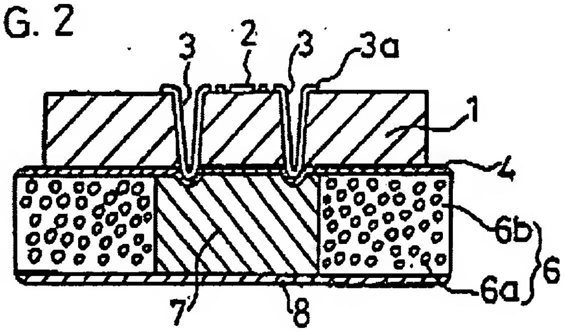
Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over all as applied to claims 1, 8, 14, 20 or 26 above, and further in view of Kosaki, US Patent 5,200,641.

FIG. 2



KOSAKI FIGURE

While none of the previous patents teach a material as recited in claim1, 8, 14, 20 or 26, further comprising at least one heat dissipation layer, Kosaki teaches the use

of a heat dissipation layer **4, 8**. It would be obvious to one skilled in the art at the time of the invention to combine the teachings of Kosaki with the teachings of any one of the others because the layer radiates heat generated by the active device (Kosaki, abstract).

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over all as applied to claims 1, 8, 14, 20 or 26 above, and further in view of Schelhorn, US Patent 4,383,270. While the others fail to explicitly teach a material as recited in claim 1, 8, 14, 20 or 26, further comprising at least one RF shield layer, Schelhorn teaches a material comprising at least one RF shield. It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Schelhorn with the teachings of any one of the others because the layer of copper provides a good RF shield for high frequency RF circuits (Schelhorn, column 4, lines 24-25).

Claims 37 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srikrishnan as applied to claims 36 and 38 above, and further in view of Matsui et al, US Patent 6,191,007. Srikrishnan fails to teach a method as recited in claims 36 and 38, further comprising planarizing said device layer, bonding said device layer to a 3-d stack or handle, injecting and diffusing hydrogen into said collection region, and ion cutting said diffusion layer at said collection region, and removing said remaining diffusion layer and insulator layer.

Matsui teaches planarizing said device layer (Figure 2D), bonding said device layer to a 3-d stack or handle (Figure 3B), injecting and diffusing hydrogen into said collection region, and ion cutting said diffusion layer at said collection region; and removing said remaining diffusion layer and insulator layer (Figure 55). It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Matsui with that of Srikrishnan because it is possible to achieve improved quality and characteristics of the semiconductor substrates and make possible the deployment of such semiconductor substrates to various uses (Matsui, abstract).

Claims 51, 57, and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al as applied to claims 45 and 52 above, and further in view of Matsui et al, US Patent 6,191,007.

Regarding claims 51 and 57, Sato fails to teach a method as recited in claims 45 and 52, further comprising planarizing said device layer, bonding said device layer to a 3-d stack or handle, injecting and diffusing hydrogen into said collection region, and ion cutting said diffusion layer at said collection region, and removing said remaining diffusion layer and insulator layer.

Matsui teaches planarizing said device layer (Figure 2D), bonding said device layer to a 3-d stack or handle (Figure 3B), injecting and diffusing hydrogen into said

collection region, and ion cutting said diffusion layer at said collection region; and removing said remaining diffusion layer and insulator layer (Figure 55). It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Matsui with that of Sato because it is possible to achieve improved quality and characteristics of the semiconductor substrates and make possible the deployment of such semiconductor substrates to various uses (Matsui, abstract).

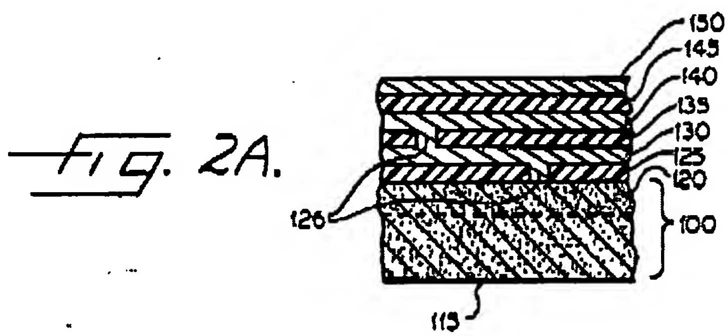
Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato as applied to claim 58 above, and further in view of Matsui et al, US Patent 6,191,007. Sato fails to teach a method as recited in claim 58, further comprising of bonding said device layer to a 3-d stack or handle, injecting and diffusing hydrogen into said collection region; and ion cutting said diffusion layer at said collection region, and removing said remaining diffusion layer and insulator layer.

Matsui teaches bonding said device layer to a 3-d stack or handle (Figure 3B), injecting and diffusing hydrogen into said collection region, and ion cutting said diffusion layer at said collection region; and removing said remaining diffusion layer and insulator layer (Figure 55). It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Matsui with that of Sato because it is possible to achieve improved quality and characteristics of the semiconductor substrates and make possible the deployment of such semiconductor substrates to various uses (Matsui, abstract).

Claim 78 is rejected under 35 U.S.C. 103(a) as being unpatentable over all as applied to claim 34, 35, 42, 43, 49, 50, 55, 56, 61, 62, 67, 68, 74 or 75 above, and further in view of Sparks, US Patent 5,719,069. While the others fail to explicitly teach the method as recited in claim 34, 35, 42, 43, 49, 50, 55, 56, 61, 62, 67, 68, 74 or 75, wherein said hydrogen getters are created by injection from a solid source adjacent said diffusion layer, Sparks teaches said hydrogen getters are created by injection from a solid source adjacent said diffusion layer (column 6, lines 27-28). It would be obvious to one skilled in the art at the time of the invention to combine the teachings of Sparks with that of any one of the others because isolation diffusions can be formed using various suitable techniques known to those skilled in the art (Sparks, column 6, lines 24-25).

Claim 79 is rejected under 35 U.S.C. 103(a) as being unpatentable over all as applied to claim34, 35, 42, 43, 49, 50, 55, 56, 61, 62, 67, 68, 74 or 75 above, and further in view of Young et al, US Patent 4,350,537. While the other inventors fail to explicitly teach a method as recited in claim 34, 35, 42, 43, 49, 50, 55, 56, 61, 62, 67, 68, 74 or 75, further comprising pulse heating said diffusion layer during injection of hydrogen getters. Young teaches pulse heating said diffusion layer during injection of hydrogen getters. It would be obvious to one skilled in the art at the time of the invention to combine the teachings of Young with that of any one of the others for annealing an ion damages semiconductor body (Young, column 1, line 30).

Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over all as applied to claim 29, 38, 45, 52, 58, 64 or 70 above, and further in view of Riesman et al, US Patent 5,168,078. See Riesman Figure.



REISMAN FIGURE

While other inventors do not explicitly teach a method as recited in claim 29, 38, 45, 52, 58, 64 or 70, further comprising forming vias and metallization to connect two or more said layers, Reisman teaches comprising forming vias and metallization to connect two or more said layers (Figure 2A). It would be obvious to one skilled in the art at the time of the invention to combine the teachings of Reisman with that of any one of the others because high density semiconductor fabrication techniques are requires for the manufacture of VLSI and USLI (Reisman, column 1, lines 18-20).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6,615,802, issued to Cuchiaro et al, discloses a method for fabricating ferroelectric integrated circuit using oxygen to inhibit and repair hydrogen degradation. US Patent 6,054,370, issued to Doyle, discloses method of delaminating a pre-fabricated transistor layer. US Patents 5,966,620 and 5,277,748, both issued to Sakaguchi et al, discloses processes for producing a semiconductor article. US Patent 6,140,210, issued to Aga et al, discloses method of fabricating an Soi wafer. US Patent 5,993,677, issued to Biasse et al, discloses a process for transferring a thin film from an initial substrate onto a final substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qvj

W. DAVID COLEMAN
PRIMARY EXAMINER